B. S. T. J. BRIEFS

Estimation of the Variance of a Stationary Gaussian Random Process by Periodic Sampling

By J. C. DALE

(Manuscript received February 14, 1967)

I. INTRODUCTION

This paper* applies previous work[1] on estimation of the mean of a stationary random process by periodic sampling to estimation of the variance with the added restriction that the process under consideration be Gaussian with known mean.

The samples are taken from a sample function of the random process, in a closed interval $(0, T)$ and are in general correlated. The estimator used is the average of equally-weighted squared samples. The variance of this estimator is derived and its behavior is predicted as a function of the number of samples and length of record.

II. THEORY

2.1 *General*

Let $x(t)$ be a sample function from a stationary, Gaussian random process $\{x(t)\}$ with known mean.†

An unbiased estimator of the variance is given by

$$\hat{\sigma}_x^2 = \frac{1}{N+1} \sum_{k=0}^{N} x^2\left(\frac{kT}{N}\right), \tag{1}$$

where T/N is the sampling period.

By invoking the Gaussian assumption, the variance of this estimator follows directly and is given by

$$\text{var } (\hat{\sigma}_x^2) = \frac{2}{N+1} \sum_{k=-N}^{N} \left(1 - \frac{|k|}{N+1}\right) R_x^2\left(\frac{kT}{N}\right),$$

* This work was supported by the U.S. Navy, Bureau of Ships under Contract N00 600-67-CO549.

† So long as the mean of $\{x(t)\}$ is assumed known, no generality of the derivation is lost by letting it be zero.

or in an equivalent form (2)

$$\text{var } (\hat{\sigma}_x^2) = \frac{2}{N+1} \int_{-\infty}^{\infty} q_{(N+1/N)T}(\tau) R_x^2(\tau) \sum_{k=-\infty}^{\infty} \delta\left(\tau - \frac{kT}{N}\right) d\tau.$$

$q_{(N+1/N)T}(\tau)$ is the triangular weighting function (See Ref. 1) and $R_x(\tau)$ is the autocorrelation function of $\{x(t)\}$.

By comparing the var $(\hat{\sigma}_x^2)$ to (3) in the previous paper[1] it is seen that (2) gives the variance of the sample mean of a stationary random process $\{x^2(t)\}$, whose autocovariance function is given by $2R_x^2(\tau)$. The spectrum of $\{x^2(t)\}$ is $2S_x(\omega) * S_x(\omega)$.

At this point the previous theory[1] applies directly. Using the same notation, the spectrum of the squared samples can be written as

$$G(\omega) = \frac{2}{N+1} \int_{-\infty}^{\infty} q_{(N+1/N)T}(\tau) R_x^2(\tau) e^{-j\omega\tau} \sum_{k=-\infty}^{\infty} \delta\left(\tau - \frac{kT}{N}\right) d\tau,$$

which is equivalent to (3)

$$G(\omega) = \frac{N}{T} \sum_{k=-\infty}^{\infty} F\left(\omega - k\,\frac{2\pi N}{T}\right).$$

In this case

$$F(\omega) = Q(\omega) * 2[S_x(\omega) * S_x(\omega)], \tag{4}$$

and $Q(\omega)$ is the transform of the weighting function.

$G(\omega)$ can be interpreted as $F(\omega)$, shifted by integral multiples of the sampling frequency, $2\pi N/T$. As before to obtain the variance of the estimate we need only be concerned with the value of $G(\omega)$ at $\omega = 0$. To minimize the variance of the estimate, the sampling frequency should be high enough to prevent overlapping of the sideband at $\omega = 0$. Satisfying this condition results in

$$\text{var } (\hat{\sigma}_x^2) = \frac{N}{T} F(0).\dagger \tag{5}$$

To answer the question of how many samples to take in time T to obtain minimum variance, consider (4). $Q(\omega)$ is approximately zero for

† Equation (5) is not quite true when both end points of the time record are included as samples. This is because $(N/T)\,F(0)$ is a function of N namely,

$$(N/T)\,F(0) = \frac{1}{2\pi} \int_{\infty}^{-\infty} 2[S_x(y) * S_x(y)] \left[\frac{\sin y(N + 1/2N)T}{y(N + 1/2N)T}\right]^2 dy.$$

Increasing N beyond the value given in (8) actually results in a higher variance on the estimate. This is apparent in the two examples, particularly for T small. This same effect was discussed in Ref. 1.

$|\omega| \geqq (2\pi/T)[N/(N+1)]$. If $S_x(\omega)$ is zero for $|\omega| \geqq 2\pi B$, then $S_x(\omega) * S_x(\omega)$ will be zero for $|\omega| \geqq 4\pi B$ and $F(\omega)$ will be approximately 0 for

$$|\omega| \geqq 2\pi\left[2B + \frac{1}{T}\left(\frac{N}{N+1}\right)\right]. \tag{6}$$

Therefore, choosing the sampling frequency so that

$$\frac{2\pi N}{T} \geqq 2\pi\left[2B + \frac{1}{T}\left(\frac{N}{N+1}\right)\right] \tag{7}$$

results in (5) being satisfied.

Solving (7) for N yields the required number of samples taken in time T to approximately minimize the variance of the estimate, namely

$$N = 2BT\left[\frac{1 + \sqrt{1 + 2/BT}}{2}\right]. \tag{8}$$

For $BT \gg 1$, N is approximately equal to $2BT$. Thus, twice the number of samples are required to obtain a minimum variance estimate of the variance than was previously shown to obtain a minimum variance estimate of the mean.

2.2 *Variance For Large T*

If T is allowed to become large $Q(\omega)$ will approach a delta function,

$$\lim_{T\to\infty} Q(\omega) = \frac{2\pi}{N+1}\,\delta(\omega). \tag{9}$$

This results in

$$F(\omega) = \frac{1}{\pi(N+1)}\int_{-\infty}^{\infty} S_x(y)S_x(\omega - y)\,dy. \tag{10}$$

If $S_x(\omega)$ is zero for $|\omega| \geqq 2\pi B$, and the sampling frequency satisfies (7), then the minimum value of variance of the estimate is given by

$$\text{var}\,(\hat{\sigma}_x^2)\Big|_{\substack{\text{min}\\ T\text{ large}}} = \frac{N}{T}F(0) = \frac{N}{T(N+1)\pi}\int_{-\infty}^{\infty} S_x^2(y)\,dy, \tag{11}$$

$$\approx \frac{1}{\pi T}\int_{-\infty}^{\infty} S_x^2(y)\,dy.$$

This is the same value obtained by continuous sampling.

III. EXAMPLES

The variance of the estimate of variance as a function of number of samples $(N+1)$ and length of record (T) has been computed for two examples.

The computation was done using an expression equivalent to (2).

3.1 *Rectangular Spectrum*

$$S_x(\omega) = \begin{cases} \frac{1}{2}; & -2\pi < \omega < 2\pi, \\ 0; & \text{elsewhere.} \end{cases} \tag{12}$$

Fig. 1 shows var $(\hat{\sigma}_x^2)$ plotted against number of samples. Each curve represents a different length of record as indicated by the values shown on tbe figure. It should be noted that the minimum value of var $(\hat{\sigma}_x^2)$ occurs at the number of samples predicted by (8). Also for small values of T the var $(\hat{\sigma}_x^2)$ reaches a minimum and then increases as more samples are taken. This is due to including hoth end points of the time record as samples.

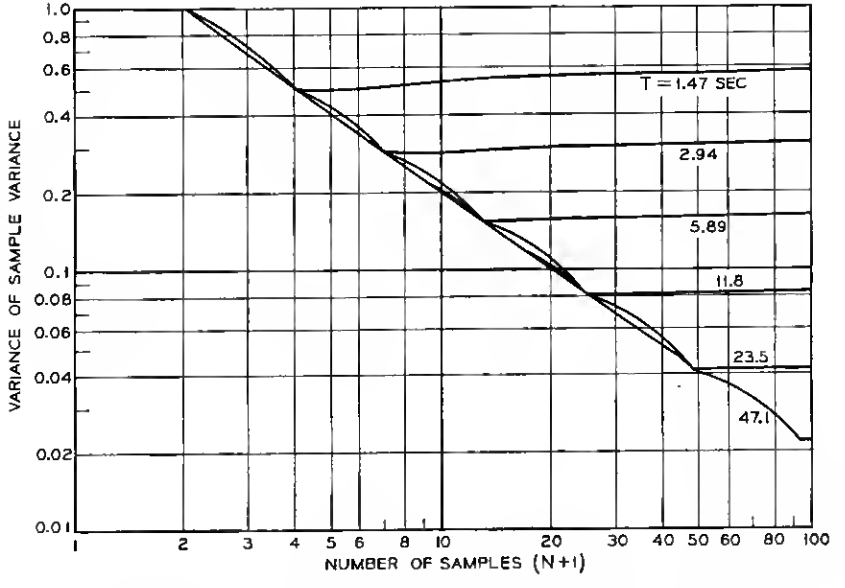

Fig. 1 — Variance of the sample variance as a function of the number of samples and length of record for a process with rectangular spectral density.

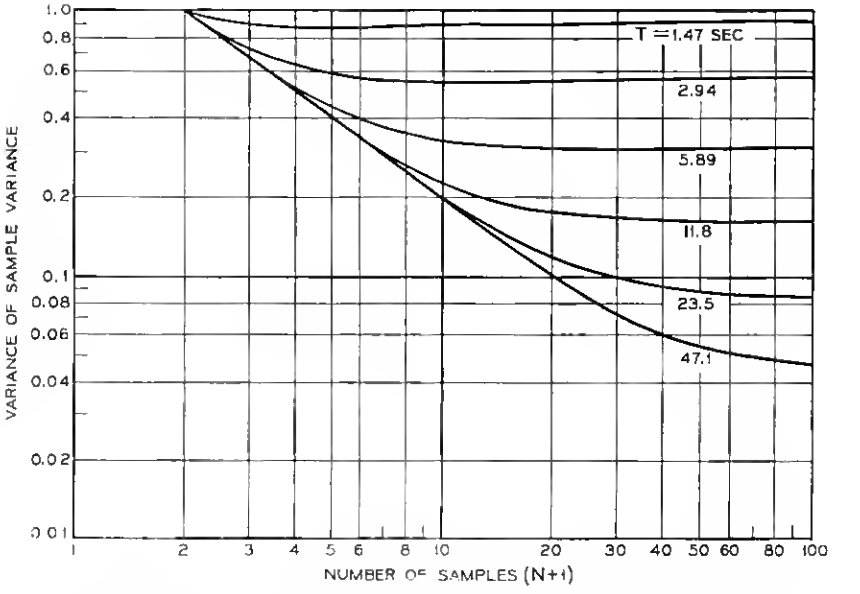

Fig. 2 — Variance of the sample variance as a function of the number of samples and length of record for a process with Markoff spectral density.

3.2 *Markoff Spectrum*

$$S_x(\omega) = \frac{2}{\omega^2 + 1}. \tag{13}$$

This sample shows a nonbandlimited spectrum. The results are shown in Fig. 2.

IV. CONCLUSION

By making the assumption that the random process $\{x(t)\}$ was Gaussian, it was possible to express var $(\hat{\sigma}_x^2)$ into an array of terms containing $R_x^2(kT/N)$, (2). In this form it is possible to apply the theory developed in the work on estimation of the mean.[1] The interesting result from this derivation was that when $BT \gg 1$, the variance of the sample variance is essentially minimized when $2BT$ samples are taken. This is in contrast to the BT samples required to minimize the variance of sample mean.

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A Floating Gate and Its Application to Memory Devices

By D. KAHNG and S. M. SZE

(Manuscript received May 16, 1967)

A structure has been proposed and fabricated in which semi-permanent charge storage is possible. A floating gate is placed a small distance from an electron source. When an appropriately high field is applied through an outer gate, the floating gate charges up. The charges are stored even after the removal of the charging field due to much lower back transport probability. Stored-charge density of the order of $10^{12}/cm^2$ has been achieved and detected by a structure similar to an metal-insulator-semiconductor (MIS) field effect transistor. Such a device functions as a bistable memory with nondestructive read-out features. The memory holding time observed was longer than one hour. These preliminary results are in fair agreement with a simple analysis.

It has been recognized for some time that a field-effect device, such as that described by Shockley and Pearson,[1] can be made bistable utilizing switchable permanent displacement charges on ferroelectric material.[2] Subsequent studies of ferroelectric material have revealed,[3] however, that the inherent speed capability of a device incorporating a ferroelectric material is limited by domain motion, whose highest speed is limited by the acoustic velocity. In the absence of highly ordered, near-ideal thin film ferroelectric material, the speed capability of a bistable device, therefore, is in the microsecond range at best.[4] In addition, many ferroelectric materials suffer from irreversible mechanical disorder after many cycles of polarization switching,[2] rendering some uncertainty on the long term device reliability aspect.

An alternative to a ferroelectric gate is a floating gate chargeable by field emission, which hopefully circumvents the above mentioned difficulties. Consider a sandwich structure, metal $M(1)$, insulator $I(1)$, metal $M(2)$, insulator $I(2)$, and finally metal $M(3)$. (See Fig. 1). If the thickness of $I(1)$ is small enough so that a field-controlled electron transport mechanism such as tunneling or internal tunnel-hopping are possible, a positive bias on $M(3)$ with respect to $M(1)$ with $M(2)$ floating [$M(2)$ is called the floating gate henceforth], would cause electron accumulation in the floating gate, provided electron transport

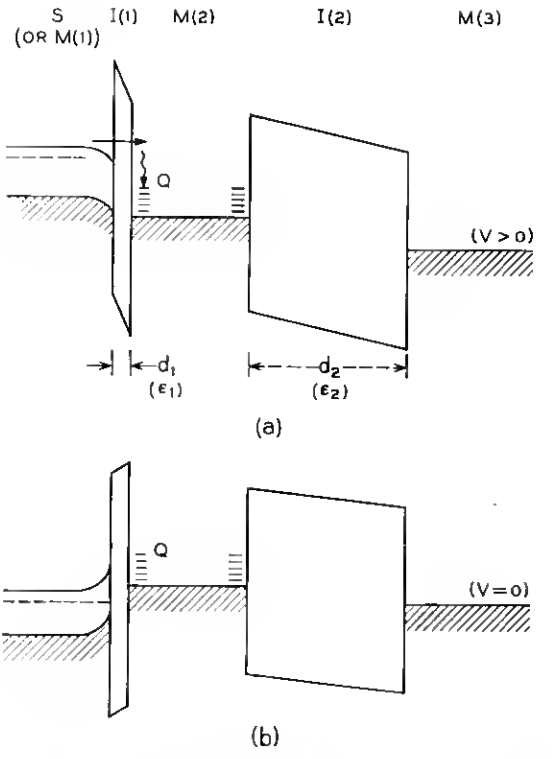


Fig. 1 — Energy band diagram of a floating gate structure with a semiconductor-insulator-metal-insulator-metal sandwich. For calculation of the stored charge, the semiconductor is replaced by a metal $M(1)$. (a) When a positive voltage step is applied to the outer gate. (b) When the voltage is removed. The stored charge Q causes an inversion of the semiconductor surface.

across $I(2)$ is small. These conditions can be met by choosing $I(1)$ and $I(2)$ such that the ratio of dielectric permittivity ϵ_1/ϵ_2 is small and/or the barrier height into $I(1)$ is smaller than that into $I(2)$. The sandwich structure is somewhat similar to the tunnel emitter metal-base transistor proposed by Mead[5] in its structure but with the following essential differences.

(*i*) $M(2)$ is much thicker than the hot electron range, so that emitted electrons are close to the Fermi-level of $M(2)$ before reaching $I(2)$.
(*ii*) No carrier transport is allowed across $I(2)$.
(*iii*) $M(2)$ is floating.

The stored charge Q, as a function of time when a step voltage function with amplitude V is applied across the sandwich, is given by

$$Q(t) = \int_0^t j\, dt' \qquad \text{coul/cm}^2. \tag{1}$$

When the emission is of Fowler-Nordheim tunneling type, then the current density, j, has the form

$$j = C_1 E^2 \exp(-E_0/E), \tag{2a}$$

where C_1 and E_0 are constants in terms of effective mass and the barrier height. (We have neglected the effects due to the image force lowering[6] of the barrier, etc., but the essential feature is expected to be retained even after detailed corrections are made). This type of current transport occurs in SiO_2 and Al_2O_3.

When the field emission is of the internal Schottky or Frankel-Poole type, as occurs in Si_3N_4,[7] then j follows the form

$$j = C_2 E \exp[-q(\Phi_1 - \sqrt{qE/\pi\epsilon_1})/kT], \tag{2b}$$

where c_2 is a constant in terms of trapping density in the insulator, Φ_1 the barrier height in volts, ϵ_1 the dynamic permittivity.

The electric field in $I(1)$ at all times is a function of the applied voltage V and $Q(t)$, and is obtainable from the displacement continuity requirement as

$$E = \frac{V}{d_1 + d_2(\epsilon_1/\epsilon_2)} - \frac{Q}{\epsilon_1 + \epsilon_2(d_1/d_2)}, \tag{3}$$

where d_1 and d_2 are the thickness of $I(1)$ and $I(2)$, respectively.

Fig. 2(a) shows the results of a theoretical computation using (1), (2a), and (3) with the following parameters: $d_1 = 50$ Å, $\epsilon_1 = 3.8\,\epsilon_0$ (for SiO_2), $d_2 = 1000$ Å, $\epsilon_2 = 30\,\epsilon_0$ (for ZrO_2), and V = 50 volts. One notes that the stored charge initially increases linearly with time and then saturates. The current is almost constant for a short time and then decreases rapidly. The field in $I(1)$ decreases slightly as the time increases. The above results can be explained as follows: When a voltage pulse is applied at $t = 0$, the initial charge Q is zero, and the initial electric field across $I(1)$ has its maximum value, $E_{max} = V/[d_1 + (\epsilon_1/\epsilon_2)d_2]$. As t increases, Q will first increase linearly with time. This is because of the fact that for small Q such that E remains essentially the same, the current will in turn remain the same, so $Q = j(E_{max}) \cdot t$. Eventually, when Q is large enough to reduce the

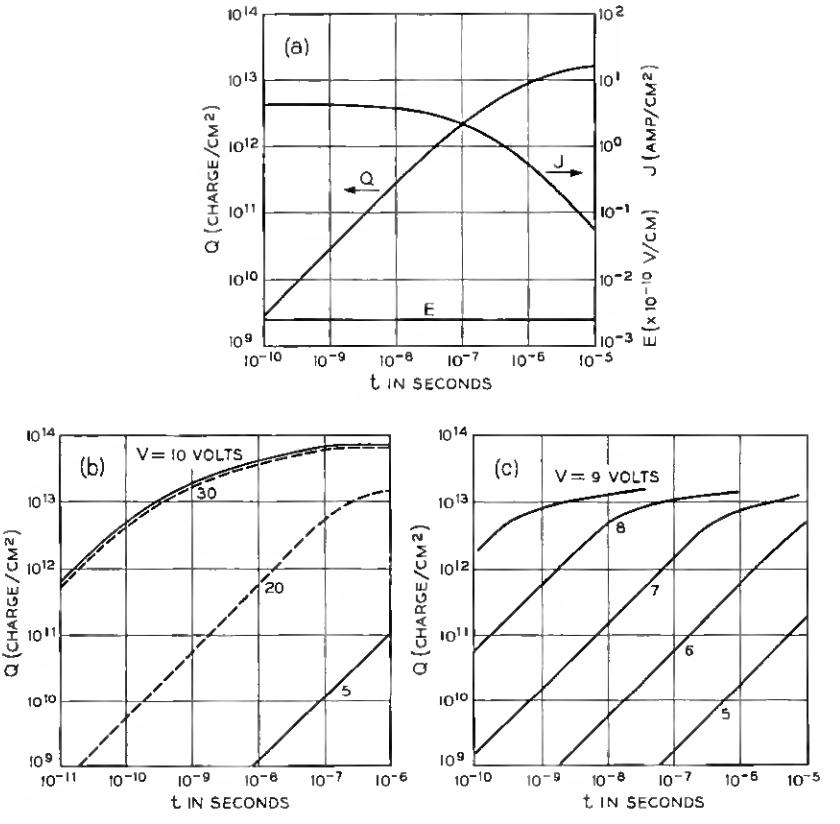


Fig. 2(a) — Theoretical results of the stored-charge density (Q), the current density (J), and the electric field across $I(1)$ as a function of time. V = 50 volts, $d_1 = 50$ Å, $\epsilon_1/\epsilon_0 = 3.8$ (for SiO_2), $d_2 = 1000$ Å, $\epsilon_2/\epsilon_0 = 30$ (for ZrO_2). (b) Theoretical results of the stored charge density as a function of time with the same ϵ_1 and ϵ_2 as in (a), and $d_1 = 10$ Å, $d_2 = 100$ Å (solid lines), $d_1 = 30$ Å, $d_2 = 300$ Å (dotted lines). (c) Theoretical results of the stored density as a function of time with $d_1 = 20$ Å, $\epsilon_1/\epsilon_0 = 60$ (for Si_3N_4), $d_2 = 200$ Å, $\epsilon_2/\epsilon_0 = 30$ (for ZrO_2) and various applied voltages.

value of E substantially, then the current will decrease rapidly with time and Q increases slowly.

Fig. 2(b) shows the stored charge as a function of time for the time ϵ_1 and ϵ_2 but different d_1, d_2, and V. It is clear that for a given structure, in order to store a given amount of charge, one can either increase the applied voltage or increase the charging time (pulse width) or both. Fig. 2(c) shows the calculated stored charge for the current transport described by (2b). Here $I(1)$ is a 20 Å thick Si_3N_4 film. There are

marked decreases in the gate voltages required for a given charge compared to Al_2O_3, SiO_2. This is largely due to the much lower barrier height (1.3 volts)[7] compared to SiO_2 ($\simeq$ 4.0 volts).[8]

It is noted that the field in $I(1)$ for appreciable charge storage is in the 10^7 V/cm range. When the outer gate voltage is removed, the field in $I(1)$ due to the stored charge on the inner gate is only 10^6 V/cm or so corresponding to 5×10^{12} charges/cm^2, a large enough charge to detect easily. Since the transport across $I(1)$ is highly sensitive to the field, (2a) and (2b), no charges flow back. The charge loss is actually controlled by the dielectric relaxation time of the sandwich structure,[9] which is very long. When it is desired to discharge the floating gate quickly, it is necessary to apply to the outer gate a voltage about equal in magnitude but opposite in polarity to the voltage which was used for charging. It is evident that net positive charges (loss of electrons) can also be stored in the floating gate if the discharging gate voltages are appropriately chosen in magnitude and duration.

It was mentioned that the stored-charge density of 5×10^{12}/cm^2 was sufficient for easy detection. One of the detection or read-out schemes is to use the surface field effect transistor (MOSFET or IGFET) first fabricated and described by Kahng and Atalla[10] in 1960. For inversion at a silicon surface, the charge required is only about 2×10^{11}/cm^2 for 1 ohm-cm n-type silicon. However, surface-state charges at the silicon-silicon dioxide interface may be as high as 10^{12}/cm^2, depending on the fabrication techniques used. For this reason we have chosen 5×10^{12}/cm^2 as the stored charge required for easy detection. When the Insulated Gate Field Effect Transistor (IGFET) principle is used for read-out, $M(1)$ is now replaced by silicon. This requires a slight correction in the calculation of charge flow through the insulator, but the major features of the results are not expected to be altered significantly. It is to be noted that about one half of the stored charge can be active in creation of the inversion layer since the other half resides near the $M(2)$-$I(2)$ interface due to Colombic repulsion.

To check the feasibility, a floating gate device has been fabricated using an IGFET as shown in Fig. 3(a). The substrate is an n-type silicon, 1 ohm-cm, and ⟨111⟩ oriented. $I(1)$ is a 50 Å SiO_2 thermally grown in a dry oxygen furnace. $M(2)$ and $I(2)$ are Zr (1000 Å) and ZrO_2 (1000 Å), respectively. $M(3)$ and the ohmic contact metals are aluminum deposited in a vacuum system. Fig. 3(b) is another version of the floating gate device using a thin film transistor (TFT) structure.[11]

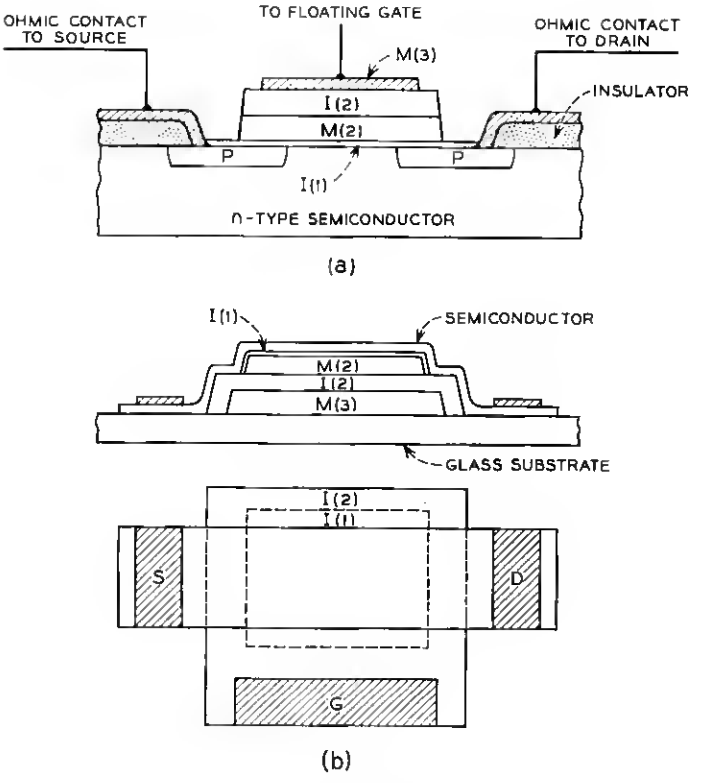
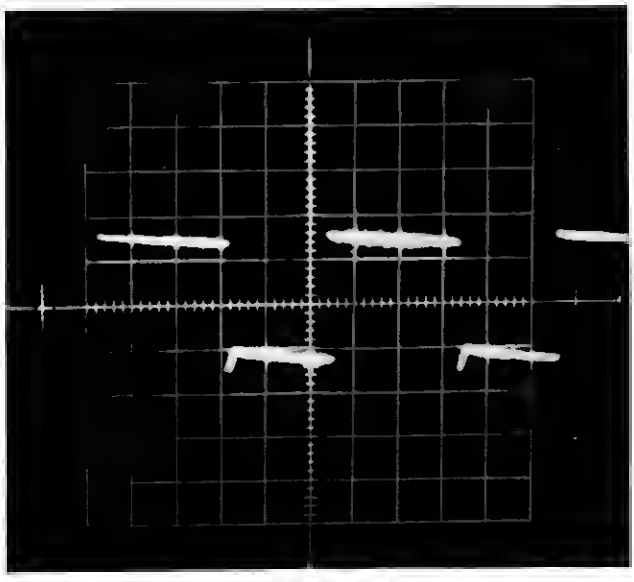
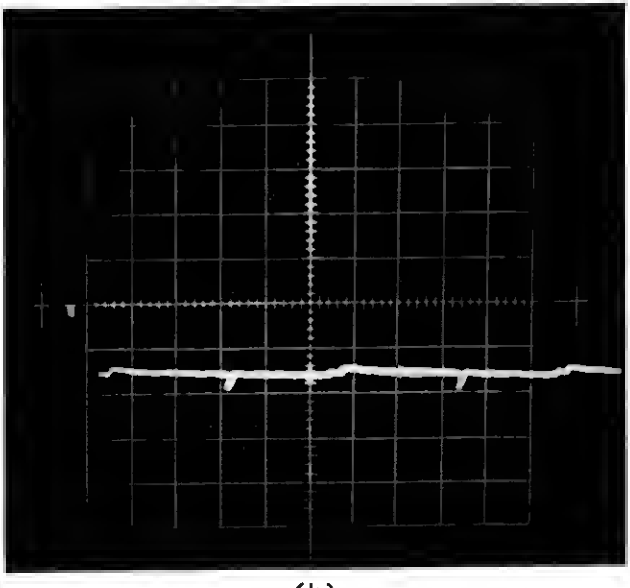


Fig. 3 — (a) Schematic diagram of a floating gate device using an IGFET. The numbers indicated correspond to those shown in Fig. 1. (b) Schematic diagram of a floating gate device using thin film transistor structure.

The IGFET-type floating gate devices have been tested in a pulsing circuit. Because of the relatively thick insulator layers, large voltages ($\approx$ 50 V) and long pulse width ($\approx$ 0.5 μs) have to be applied in order to store $\approx 5 \times 10^{12}$ charges/cm^2. Fig. 4 shows the experimental results. A positive pulse of 50 volts is first applied to the gate electrode, and 60 ms later a negative pulse of 50 volts is applied. Then the pulsing cycle repeats. In Fig. 4(a) the pulse widths are 0.5 μs. One notes that when the positive pulse is applied, a sufficient amount of charge is stored in the floating gate so that the silicon surface is inverted; a conducting channel is thus formed, and the channel current is "on." It can be seen that the channel current decreases only slightly at the end of 60 ms. When the negative pulse is applied, the stored charge is eliminated, and also the channel. The channel current reduces to its



(a)



(b)

Fig. 4 — Experimental results of the channel current of a IGFET-type floating gate device. A positive voltage pulse, V_1, with pulse width W_1, is first applied to the gate, and 60 ms later a negative pulse V_2 with pulse width W_2 is applied. Then the pulsing cycle repeats. Horizontal scale: 20 ms/div. Vertical scale: 0.1 ma/div. (a) $V_1 = V_2 = 50$ volts, $W_1 = W_2 = 0.5$ μs. (b) $V_1 = V_2 = 40$ volts, $W_1 = W_2 = 0.5$ μs.

"off" state. Fig. 4(b) shows results for pulses with the same widths but smaller amplitude (40 V). Since the stored charge is a strong function of the pulse amplitude, only a very small amount of charge is stored, too small to cause inversion. For non-leaky units, the memory holding time of longer than one hour has been observed.

It is clear that a modified IGFET such as a TFT can be used for read-out, as shown in Fig. 3(b). For an academic study of device operation, the floating gate can be partially exposed and a potential probe can be placed nearby.

In conclusion, it has been demonstrated that the controlled field emission to the buried "floating" gate may be capacitively induced by pulsing the outer gate electrode. This combination can therefore, be used as a memory deviee, with holding time as long as the dieleetrie relaxation time of the gate structure and with continuous nondestructive read-out capability. There seems to be no inherent reason why read-in read-out cannot be performed in a very short time, say in the nanosecond range or even shorter.

We wish to acknowledge helpful discussions and technical assistance rendered by M. P. Lepselter and P. A. Byrnes in connection with ZrO_2, and skillful technical assistance given to us by G. P. Carey and A. Loya, and J. F. Grandner and his group.

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Semipermanent Memory Using Capacitor Charge Storage and IGFET Read-out

By D. KAHNG

(Manuscript received May 17, 1967)

One of the earliest computers used capacitors as its memory.[1] A mechanical means was used for both read-in and read-out operations. Electronic accessing was used in conjunction with vacuum tube or solid-state diodes in relatively modern computers such as the SEAC computer.[2] Capacitor storage is rarely used at present since magnetic memories meet the modern computer requirements much better. The inherent difficulty with capacitor storage was the limited holding time since a nonlinear resistor with small enough leakage currents to allow useful memory holding time was then not readily available. The old capacitor memory was charged through a diode with slow recovery time and with leakage current of 10^{-10} amp at best and required a large capacitor for any appreciable holding time. Furthermore, the read-out was usually destructive.

The capacitor storage merits re-examination in view of the advanced solid-state devices and technology now available. Coupled with an Insulated Gate Field Effect Transistor (IGFET),[3] the read-out can be nondestructive. Integrated circuit techniques may prove superior to the current magnetic memories for some applications where infrequent recycling is permissible. The inherent speed should be much faster than that of magnetic units.

Consider a capacitor C in series with a nonlinear element as shown in Fig. 1. The capacitor may represent the gate capacity of the IGFET plus any external capacitor in parallel with the gate capacitor. When a positive voltage pulse with amplitude V and duration τ is applied at the nonlinear element terminal, it can be shown that the stored charge $Q(\tau)$ and the decay time constant τ_e, defined as the time required to reach $1/e$ value of the initial stored charge Q_o, can be calculated for various nonlinear resistors.

I. POWER-LAW RESISTORS

The I-V characteristics are given by

$$I = KV_n^m, \tag{1}$$

then

$$Q(\tau) = C\left[V - \left(\frac{1}{V^{(m-1)}} + K(m-1)\frac{\tau}{C}\right)^{-1/(m-1)}\right] \tag{2}$$

and

$$\begin{aligned}\tau_e &= \frac{C^m}{(m-1)K}\frac{1}{Q_0^{(m-1)}}(e^{(m-1)} - 1) \\ &= \frac{(e^{(m-1)} - 1)}{(m-1)}\frac{Q_0}{I_0},\end{aligned} \tag{3}$$

where I_0 is the discharge current at the termination of charging. It is clear from (2) that m $\geqq$ 1 for physically meaningful $Q(\tau)$. For a long holding time, (3) tells us that the nonlinearity of the resistor should be large. These equations would describe the behavior of the storage unit comprising a space-charge-limited-current diode.[4] If traps are present, only a simple modification is needed in the analysis. Structures comprising photosensitive space-charge-limited-current diodes such as CdS diodes should allow optical read-in operations which might be advantageous for certain applications such as a vidicon.

II. TUNNEL SANDWICH DIODES

For this nonlinear element, the circuit in Fig. 1 should be modified to include the shunt capacitance of the tunnel sandwich. Thus, at the instance of pulse application, the voltage divides between the two capacitors. The I-V relationship for Fowler-Nordheim type tunneling is

$$I = KV_n^2 e^{-V_0/V_n}. \tag{4}$$

With the appropriate initial conditions, the stored charge $Q(\tau)$ is given by

$$Q(\tau) = C\left[V - \alpha V_0/\ln\left(e^{\alpha V_0/V} + \frac{KV_0}{C}\tau\right)\right], \tag{5}$$

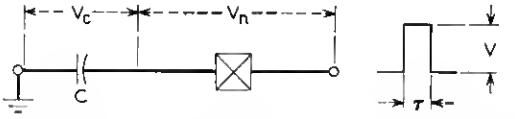

Fig. 1 — A capacitor being charged through a nonlinear resistor.

where α is defined as unity plus the ratio of the shunt capacitance of the tunnel sandwich, C_n to the charging capacitor, namely $\alpha = 1 + (C_n/C)$.

The discharge time constant τ_e can also be shown to be

$$\tau_e = \frac{\frac{\alpha C}{KV_0}\left(e^{(\alpha CV_0/Q_0)(e-1)} - 1\right)}{e^{\alpha CV_0/Q_0}} = \tau_c e^{(\alpha CV_0/Q_0)(e-2)}. \tag{6}$$

It is clear that charging time required for adequately large Q is very short, allowing fast read-in operation. The decay time can be seen to be large for tunneling across well-known insulators such as SiO_2 and Al_2O_3. Therefore, the decay is not controlled by (6) but rather by tbe dielectric relaxation time of the insulators used for the entire assembly including the IGFET gate material. The dielectric relaxation time of the best inorganic insulators is of the order of one day at room temperatures. However, certain organic insulators are known to have theoretical dielectric relaxation times of many years. Performance of a memory cell incorporating a tunnel sandwich diode is described in more detail elsewhere.[5]

III. SCHOTTKY BARRIER DIODES

For charging through a rectifier, Schottky barrier diodes are preferred over pn junction diodes since Schottky barriers are majority carrier devices and hence fast recovery is achievable.[6] I-V characteristics may be represented by

$$I = I_s(e^{\beta V} - 1). \tag{7}$$

For charging, we may neglect the unity in the bracket in (7), and the stored charge can be shown to be

$$Q(\tau) = C\left[V - \frac{1}{\beta}\ln\left(\frac{\tau}{\tau_c} + e^{-\beta V}\right)^{-1}\right], \tag{8}$$

where

$$\tau_c = \frac{C}{\beta I_s}.$$

For decay, it is easy to show

$$\tau_e = \frac{Q_0}{I_s}(1 - e^{-1}). \tag{9}$$

Fig. 2 shows the stored charge Q computed from (8) as a function of pulse duration for several pulse amplitudes. The characteristic time constant τ_c is not much less than 1 sec for a typical configuration ($C < 10^{10}$ Fd, $I_s > 10^{-12}$ amp). Therefore, it is seen that the stored charge is proportional to the pulse amplitude for sufficiently large V. This suggests that the device may be used as a multi-level storage unit.

The combination of Schottky barrier diodes and the IGFET is shown in Fig. 3. A similar structure has been fabricated and tested. The holding time was of the order of 10 sec when the charging was done by 15 volts pulse in agreement with (9) since the IGFET gate capacitance was about 10^{-12} Fd and I_s of the diode was 10^{-12} amp (measured at 10 volts reverse bias). The maximum pulse amplitude before the breakdown of the gate insulator was about 30 volts, allowing a longer holding time of about 30 seconds. The read-in time was less than 10^{-7} second and the reverse breakdown of the diode was used to turn the IGFET off, which also took less than 10^{-7} second.

A memory featuring nondestructive read-out, access times in the

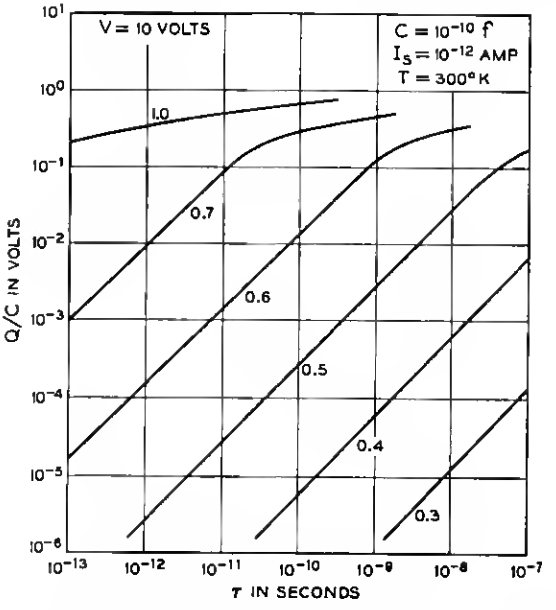

Fig. 2 — Theoretical stored charge/storing capacitance (the floating potential) as a function of time for charging through a Schottky barrier diode.

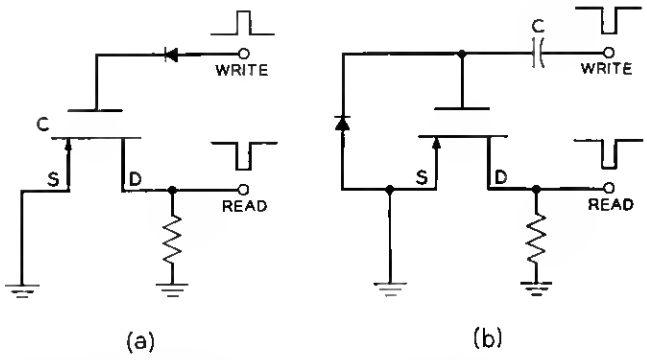

Fig. 3 — Combination of the capacitor storage unit with a p-channel IGFET for read-out. (a) Series connection, read-in should be positive. (b) Parallel connection, read-in should be negative.

submicrosecond range, and holding times of many seconds should find many applications. An integrated structure incorporating Schottky barrier diodes and IGFETs is readily obtainable with modern solid-state technology.

IV. ACKNOWLEDGMENT

The author gratefully acknowledges helpful discussions he had with H. K. Gummel, R. M. Ryder, J. E. Iwersen, and S. M. Sze.

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